



Information Disclosure Statement by Applicant <i>(use as many sheets as necessary)</i>				<i>Complete if Known</i>	
				<i>Application Number</i>	10/721,573
				<i>Filing Date</i>	November 24, 2003
				<i>First Named Inventor</i>	Low Yau Loong
				<i>Art Unit</i>	2825
				<i>Examiner Name</i>	Unassigned <i>P. RIK</i>
Sheet	1	of	1	<i>Attorney Docket Number</i>	015114-068900US

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		
<i>PR</i>	1	"Command Line Scripting," <i>Quartus II Handbook Volume 2, Design Implementation & Optimization</i> , ch. 2, pp. 1-19, Altera Corporation 101 Innovation Drive San Jose, CA (2004).		²
<i>PR</i>	2	"Quartus II Integrated Synthesis," <i>Quartus II Handbook Volume 1, Design & Synthesis</i> , ch. 8, pp. 1-28, Altera Corporation 101 Innovation Drive San Jose, CA, pp. 8-1 to 8-28,		
<i>PR</i>	3	"Quartus Programmable Logic Development System & Software," product Data Sheet, May 1999, ver. 1.01, Altera Corporation 101 Innovation Drive San Jose, CA (1999), pp. 1-16.		
<i>PR</i>	4	CHEN et al. "Performance-Driven Mapping for CPLD Architecture", Proc. ACM/SIGDA International Symposium on Field Programmable Gate Arrays, Monterey, California February 2001, pp. 39-47 (2001).		

Examiner Signature	<i>Ghallak</i>	Date Considered	<i>10/27/05</i>
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.